

We claim:

1. An integrated circuit for use in a transceiver module, the integrated circuit comprising:
a first electrical input port for receiving a first serial electrical data stream;
receiver eye opener circuitry including components for retiming and reshaping the first serial electrical data stream;
a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;
a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit;
transmitter eye opener circuitry including components for retiming and reshaping the second serial electrical data stream;
a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream; and
loopback circuitry for switchably forming a loopback data path, the loopback data path comprising a loopback between a point on a receive path and a point on a transmit path, wherein the receive path is from the first electrical input port through the receiver eye opener circuitry to the first electrical output port and the transmit path is from the second electrical input port through the transmitter eye opener circuitry to the second electrical output port.
2. The integrated circuit of claim 1 wherein the loopback data path is from the second electrical input port to the first electrical output port.
3. The integrated circuit of claim 2 wherein the loopback is from a point located between the second electrical input port and the retiming and reshaping components of the transmitter eye opener circuitry to a point located between the retiming and reshaping components of the receiver eye opener circuitry and the first electrical output port.

4. The integrated circuit of claim 1 wherein the loopback data path is from the first electrical input port to the second electrical output port.
5. The integrated circuit of claim 4 wherein the loopback is from a point located between the first electrical input port and the retiming and reshaping components of the receiver eye opener circuitry to a point located between the retiming and reshaping components of the transmitter eye opener circuitry and the second electrical output port.
6. The integrated circuit of claim 1 wherein the loopback data path includes the retiming and reshaping components of the receiver eye opener circuitry but not the retiming and reshaping components of the transmitter eye opener circuitry.
7. The integrated circuit of claim 1 wherein the loopback data path includes the retiming and reshaping components of the transmitter eye opener circuitry but not the retiming and reshaping components of the receiver eye opener circuitry.
8. The integrated circuit of claim 1 wherein the loopback data path includes some of the retiming and reshaping components of the transmitter eye opener circuitry and other of the retiming and reshaping components of the receiver eye opener circuitry, wherein the loopback data path includes a same retiming and reshaping functionality as the eye opener circuitry.
9. The integrated circuit of claim 1 further comprising:
loopback control circuitry coupled to the loopback circuitry for controlling the loopback circuitry to form the loopback data path.
10. The integrated circuit of claim 1 further comprising:
power management circuitry for powering down the loopback circuitry when the loopback data path is not formed.

11. In an integrated circuit for use in a transceiver module, a method of creating a loopback data path comprising, within the integrated circuit:

receiving a signal from external to the integrated circuit on a first path, the first path being either a receive path or a transmit path, wherein the receive path is from a first electrical input port through receiver eye opener circuitry to a first electrical output port and the transmit path is from a second electrical input port through transmitter eye opener circuitry to a second electrical output port;
forming a loopback between a point on the receive path and a point on the transmit path;
and
transmitting the signal to external to the integrated circuit from a second path, the second path being the other of the receive path and the transmit path.

12. An integrated circuit for use in a transceiver module, the integrated circuit comprising:
first input means for receiving a first serial electrical data stream;

first eye opener means for retiming and reshaping the first serial electrical data stream;

first output means for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;

second input means for receiving a second serial electrical data stream from external to the integrated circuit;

second eye opener means for retiming and reshaping the second serial electrical data stream;

second output means for transmitting the retimed and reshaped second serial electrical data stream; and

loopback means for switchably forming a loopback between a point on a receive path and a point on a transmit path, wherein the receive path is from the first input means through the first eye opener means to the first output means and the transmit path

is from the second input means through the second eye opener means to the second output means.

13. An integrated circuit for use in a transceiver module, the integrated circuit comprising:
 - a first electrical input port for receiving a first serial electrical data stream;
 - receiver eye opener circuitry including components for retiming and reshaping the first serial electrical data stream;
 - a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;
 - a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit;
 - transmitter eye opener circuitry including components for retiming and reshaping the second serial electrical data stream;
 - a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream; and
 - a bit error rate tester (BERT) engine for testing a test data path from a starting test point to an ending test point, the starting test point and the ending test point each located on either a receive path or on a transmit path, wherein the receive path is from the first electrical input port through the receiver eye opener circuitry to the first electrical output port and the transmit path is from the second electrical input port through the transmitter eye opener circuitry to the second electrical output port.
14. The integrated circuit of claim 13 wherein the test data path includes the retiming and reshaping components of the receiver eye opener circuitry.
15. The integrated circuit of claim 13 wherein the test data path includes the retiming and reshaping components of the transmitter eye opener circuitry.

16. The integrated circuit of claim 13 wherein the test data path includes the second electrical output port and the first electrical input port.
17. The integrated circuit of claim 16 wherein:
the starting test point is located between the retiming and reshaping components of the transmitter eye opener circuitry and the second electrical output port; and
the ending test point is located between the first electrical input port and the retiming and reshaping components of the receiver eye opener circuitry.
18. The integrated circuit of claim 13 wherein each of the starting test point and the ending test point is located between the first electrical input port and the retiming and reshaping components of the receiver eye opener circuitry, between the retiming and reshaping components of the receiver eye opener circuitry and the first electrical output port, between the second electrical input port and the retiming and reshaping components of the transmitter eye opener circuitry, or between the retiming and reshaping components of the transmitter eye opener circuitry and the second electrical output port.
19. The integrated circuit of claim 13 wherein the BERT engine generates a test pattern at a data rate of at least approximately 10 Gb/s.
20. The integrated circuit of claim 13 wherein the BERT engine comprises:
pattern generator circuitry coupled to the starting test point, for generating a test pattern for testing the test data path; and
error detector circuitry coupled to the ending test point, for detecting errors in the test pattern.
21. The integrated circuit of claim 13 further comprising:
BERT control circuitry coupled to the BERT engine for controlling testing of the test data path.

22. The integrated circuit of claim 13 further comprising:
power management circuitry for powering down the BERT engine when no testing of the
test data path is occurring.
23. In an integrated circuit for use in a transceiver module, a method of testing a data path
comprising, within the integrated circuit:
generating a test pattern;
injecting the test pattern at a starting test point; and
receiving the test pattern at an ending test point;
wherein the starting test point and the ending test point are each located on either a
receive path or on a transmit path, wherein the receive path is from a first
electrical input port through receiver eye opener circuitry to a first electrical
output port and the transmit path is from a second electrical input port through
transmitter eye opener circuitry to a second electrical output port.
24. The method of claim 23 wherein the test pattern has a data rate of at least approximately
10 Gb/s.
25. The method of claim 23 further comprising:
detecting errors in the test pattern received at the ending test point.
26. An integrated circuit for use in a transceiver module, the integrated circuit comprising:
first input means for receiving a first serial electrical data stream;
first eye opener means for retiming and reshaping the first serial electrical data stream;
first output means for transmitting the retimed and reshaped first serial electrical data
stream to external to the integrated circuit;
second input means for receiving a second serial electrical data stream from external to
the integrated circuit;

second eye opener means for retiming and reshaping the second serial electrical data stream;

second output means for transmitting the retimed and reshaped second serial electrical data stream; and

BERT testing means for testing a test data path from a starting test point to an ending test point, the starting test point and the ending test point each located on either a receive path or on a transmit path, wherein the receive path is from the first input means through the first eye opener means to the first output means and the transmit path is from the second input means through the second eye opener means to the second output means.